UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,556	02/25/2002	Dirk Hottgenroth	P2001,0129	3140

24131 7590 12/03/2004

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,556	HOTTGENROTH, DIRK	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed September 14, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Claims 1-17 are presented for examination.

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is required in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunziata (United States Patent 5,619,471) in view of Kerstein et al. (United States Patent 6,021,478), hereinafter Kerstein.

As per claims 1 and 17, Nunziata discloses in FIG. 2 a method for operating an integrated memory unit comprises: receiving addresses and access data from outside the integrated memory unit with the common external terminal pin; before a memory access, partitioning the memory cell field (Bank 0 – Bank 3) into a plurality of memory areas (e.g. column 10, lines 3-9); for a memory access, selecting one of the memory areas by applying a memory area address (e.g. column 5, lines 22-35); during the memory access,

internally generating addresses with the memory unit for the access to memory cells of one of the memory areas (inherent); and transmitting the memory area address, and, subsequently and successively, transmitting access data of the one of the memory areas through the common external terminal pin of the integrated memory unit (e.g. column 4, lines 1-6). However, Nunziata fails to teach for internally generating addresses with a counter of the integrated memory. Kerstein teaches that the address of subsequent data bytes can be generated by the integrated memory (FIG. 5, 51) by advancing or incrementing its internal address counter to reduce design cost and logic complexity by eliminating unnecessary pins (column 2, lines 14-41). Accordingly, it would have been prima facie obvious for one skilled in the art at the time the invention was made to implement the method for operating an integrated memory as taught by Nunziata and apply Kerstein's address generation method to generate the claimed invention with a reasonable expectation of success. One skilled in the art would have been motivated to do so for the reasons set forth above.

As per claim 2, Nunziata discloses the method further comprises transmitting, with an initialization command, one of a number to be determined of the memory areas; and a size of the memory areas (e.g. FIG. 1, column 10, lines 3-7 *"At initialization of the system, the microprocessor **10**... determine the size of DRAM banks..."*).

As per claim 3, Nunziata discloses the method further comprises transmitting one of a number of the memory areas and a size of the memory areas, with an initialization

command (e.g. FIG. 1, column 10, lines 3-7 *"At initialization of the system, the microprocessor **10**... determine the size of DRAM banks..."*).

As per claim 4, Nunziata discloses the further comprises: transmitting a start address for the memory access; and beginning with the start address, generating addresses for the access to the memory cells of the one of the memory areas (e.g. column 5, lines 22-35).

As per claim 5, Nunziata discloses a system method for controlling DRAM of a digital data processing device (e.g. column 1, lines 13-15). Thus, the method for transmitting an interrupt command for one of an interruption and a termination of the memory access at a time defined by the interrupt command is inherent in order to provide direct memory access (DMA) to the processing device.

As per claim 6, Nunziata discloses the method further comprises: applying a selection signal to the memory unit (e.g. column 5, lines 31-35); and transmitting at least two commands for the memory access by the application of the selection signal to the memory unit (e.g. column 5, lines 36-41).

As per claim 7, Nunziata discloes the method further comprises transmitting a readout command and a write command through the selection signal (e.g. column 5, lines 36-41).

As per claims 8-9, Nunziata discloses a system method for controlling DRAM of a digital data processing device (e.g. column 1, lines 13-15). Thus, the method for transmitting at least one of an initialization command, an interrupt command, and a masking signal through the selection signal inherent in order to provide direct memory access (DMA) to the processing device.

As per claim 10, Nunziata discloses the method further comprises applying an activation signal (FIG. 2, CASE[3:0] and CASO[3:0]) to each of the memory units for an activation of the respective memory unit given an operation of a plurality of memory units at a common data bus (e.g. column 5, lines 31-36).

As per claim 11, Nunziata discloses the method further comprises additionally utilizing the activation signal as a timing signal for operation of the respective memory unit (e.g. column 5, lines 31-36).

As per claim 12, Nunziata discloses the method further comprises simultaneously utilizing the activation signal as a timing signal for operation of the respective memory unit (e.g. column 5, lines 31-36).

As per claim 13, Nunziata discloses the method further comprises: operating memory units at a common data bus (inherent); and applying an activation signal to each of the

memory units for an activation of the respective one of the memory units (e.g. column 5, lines 31-36).

As per claim 14, Nunziata discloses the method further comprises additionally utilizing the activation signal as a timing signal for operation of the respective memory unit (e.g. column 5, lines 31-36).

As per claim 15, Nunziata discloses the method further comprises simultaneously utilizing the activation signal as a timing signal for operation of the respective memory unit (e.g. column 5, lines 31-36).

As per claim 16, Nunziata discloses the method substantially as claimed including executing the partitioning step, the selecting step, the internally generating step, and the transmitting step as detailed in claimed 1. However, Nunziata does not particularly disclose a test mode for testing the functionality of the memory unit. Official notice is taken that a test mode for testing the functionality of a memory unit is notoriously well known. It would have been obvious for one skilled in the art at the time the invention was made to implement the system and method as taught by Nunziata and to include a test mode for testing the functionality of the memory unit. One skilled in the art would motivate to do so, because the test mode provides a system with the detection and notification of a memory failure insuring data integrity of the memory unit thereby, preventing the system from operate in a malfunction state.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 571-272-4206. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 3:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 11/29/04

Thang Ho
Art Unit 2188
November 22, 2004

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER